PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMG/17/10392

Analog & MEMS Group (AMG)

New set of material in Amkor Philippines for TSSOP14 and TSSOP16 packages

WHAT:

Progressing on the activities related to quality continuous improvement, ST is glad to announce a new material set (molding compound) for products in TSSOP14 and TSSOP16 packages produced in Amkor Philippines.

Besides, we will introduce a new lead-frame (XDLF) with higher density in order to increase our production capacity and rationalize our production tool. This change implies the phase out of the Old Lead Frame Matrix (OMLF) and High Density Lead Frame (HDLF), and it has no impact on the internal lead-frame structure.

This PCN applies to Standard commercial products.
Please find here below more information related to this change:

Material	Current process	Modified process	Comment
Diffusion location	No change		
Assembly location	Amkor Philippines		
Molding compound	SUMITOMO EME-G700K	Sumitomo G700LS	
Die attach	ABLEBOND 8290		
Leadframe	Copper OMLF/HDLF	Copper XDLF	Higher number of unit per leadframe during production
Wire	Gold 1 mil		
Plating	Sn		
MSL	No change		

Samples of vehicle tests are available now and other samples will be launched upon customer's requests. Please submit requests for samples within 30 days of this notification.

WHY:

The change of the molding compound (from Sumitomo G700K to Sumitomo G700LS) will improve our quality level and the higher density lead-frame will allow a greater efficiency and productivity.

HOW:

•The change affects molding compound and lead frame strip density. The qualification is based on representative Test vehicles, using internal ST rules for changes.
•To validate the change, dedicated engineering trials have been performed and reliability report is attached.

WHEN:

The estimated date for the first shipment is wk41 2017.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.
There is -as well- no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

Shipments may start earlier with the customer's written agreement.

Reliability Report

TSSOP14- 16 material set change
Amkor Philippines

General Information	
Product Line	*R365, R851, 0124, UP06, UP04*
Product Description	Hex bus buffer with 3-state outputs, Single 8-channel analog MUX/DEMUX, Quad op amp, DC-DC PWM ctrl+POE Interface, LED Display Driver
P/N	*M74HC365PT, M74HC4851PT, LM2902PT, SUP06, STAP08DP05XTTR*
Product Group	*AMG*
Product division	*General Purpose Analog &RF, Industrial& Power Conversion*
Package	*TSSOP16, TSSOP14, HTSSOP16*
Silicon Process technology	*High speed CMOS, HCMOS4, BCD6S, BCD6*

Locations	
Wafer fab	*ST Singapore Catania*
Assembly plant	*Amkor ATP1*
Reliability Lab	*ST Catania, ST Grenoble, Casteletto*

Reference : REL.6088-146 W-17 : Reliability Evaluation Report Automotive Qualification Grade 1
Assy & TnF transfer from BOUSKOURA to AMKOR Package TSSOP16, T.V1.: M74HC4365, T.V2: M74HC4851

RR001917CS6080: Reliability UP06

REL-6088-127-W-17: Reliability report STAP08DP5XTTR

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
0061692	Reliability tests and criteria for qualifications

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify a new material set (molding compound sumitomo G700LS) for products in TSSOP14 and TSSOP16 package produced in Amkor Philippines.

3.2 Conclusion

Qualification Plan requirements will have to be fulfilled without issue. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

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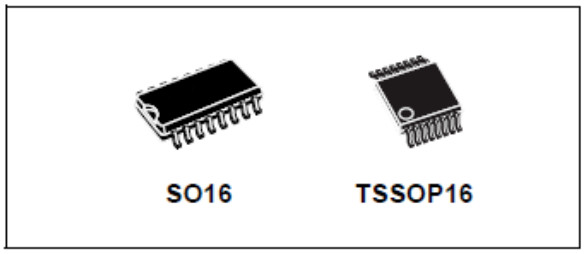
M74HC365

Hex bus buffer with 3-state outputs (non-inverting)

Datasheet - production data



Features

- High-speed:
  t_{PD} = 10 ns (typ.) at V_{CC} = 6 V
- Low power dissipation:
  I_{CC} = 4 µA (max.) at T_A = 25 °C
- High noise immunity:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (min)
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 6 mA (min.)
- Balanced propagation delays:
  $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range:
  V_{CC} (opr) = 2 V to 6 V
- Pin and function compatible with 74 series 365
- ESD performance
  - HBM: 2 kV
  - MM: 200 V
  - CDM: 1 kV

Description

The M74HC365 is an advanced high-speed CMOS hex bus buffer (3-state) fabricated with silicon gate C^2MOS technology.

All six buffers are controlled by the combination of two enable inputs ($\overline{G1}$ and $\overline{G2}$). All outputs of these buffers are enabled only when both $\overline{G1}$ and $\overline{G2}$ inputs are held low. Under all other conditions these outputs are disabled in a high-impedance state.

The M74HC365 has non-inverting outputs.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Order code	Temp. range	Package	Packing	Marking
M74HC365RM13TR	-55 °C to 125 °C	S016	Tape and reel	74HC365
M74HC365YRM13TR(1)	-40 °C to 125 °C	SO16 (automotive grade)		74HC365Y
M74HC365TTR	-55 °C to 125 °C	TSSOP16		HC365
M74HC365YTTR(1)	-40 °C to 125 °C	TSSOP16 (automotive grade)		HC365Y

M74HC4851

Single 8-channel analog MUX/DEMUX with injection current protection

Datasheet – production data

Features

- Low power dissipation
  - I_{CC} = 2 µA (max.) at T_A = 25 °C
- Injection current protection
  - $V_{\Delta OUT}$ < 1 mV at V_{CC} = 5 V, I_{IN} ≤ 1 mA
  - R_S ≤ 3.9 kΩ
- "ON" resistance at T_A = 25 °C
  - 215 Ω typ. (V_{CC} = 3.0 V)
  - 160 Ω typ. (V_{CC} = 4.5 V)
  - 150 Ω typ. (V_{CC} = 6 V)
- Fast switching
  - t_{pd} = 8.6 ns (typ.) at T_A = 25 °C, V_{CC} = 4.5 V
- Wide operating supply voltage range
  - V_{CC} = 2 V to 6 V
- High noise immunity
  - V_{NIH} = V_{NIL} = 28% V_{CC} (min.)
- Pin and function compatible with series 4051, 4851
- Latch-up performance exceeds 500 mA
  - (JESD 17)
- ESD performance
  - HBM: 2000 V
  - MM: 200 V
  - CDM: 1000 V

SO-16

TSSOP16

Applications

- Automotive
- Computer
- Consumer
- Industrial

Description

The M74HC4851 device is a single 8-channel analog multiplexer/demultiplexer manufactured with silicon gate C^2MOS technology.

It features injection current effect control which makes the device particularly suited for use in automotive applications where voltages in excess of normal logic voltages are common. The injection current effect control allows signals at disabled input channels to exceed the supply voltage range or go down to ground without affecting the signal of the enabled analog channel.

This eliminates the need for external diode-resistor networks typically used to keep the analog channel signals within the supply voltage range.

Table 1. Device summary

Order code	Temperature range	Package	Packaging	Marking
M74HC4851YRM13TR(1)	-40/+125 °C	SO-16 (automotive grade)	Tape and reel	74HC4851Y
M74HC4851RM13TR	-55/+125 °C	SO-16	Tape and reel	74HC4851
M74HC4851YTTR(1)	-40/+125 °C	TSSOP16 (automotive grade)	Tape and reel	HC4851Y
M74HC4851TTR	-55/+125 °C	TSSOP16	Tape and reel	HC4851

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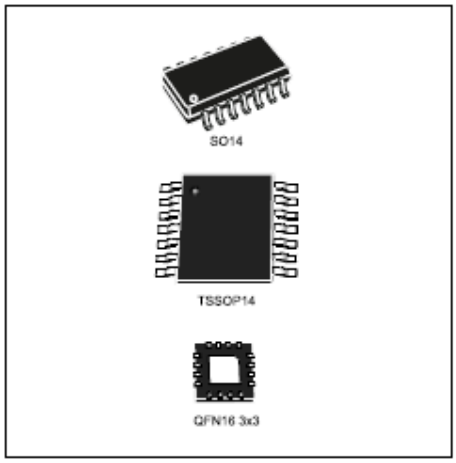
LM2902

Low-power quad operational amplifiers

Datasheet - production data



Description

This circuit consists of four independent, high-gain operational amplifiers (op amps) which employ internal frequency compensation and are specifically designed for automotive and industrial control systems.

The device operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low-power supply current drain is independent from the power supply voltage magnitude.

Features

- Wide gain bandwidth: 1.3 MHz
- Input common-mode voltage range includes negative rail
- Large voltage gain: 100 dB
- Supply current per amplifier: 375 µA
- Low input bias current: 20 nA
- Low input offset current: 2 nA
- Wide power supply range:
  - Single supply: 3 V to 30 V
  - Dual supplies: ± 1.5 V to ± 15 V

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STAP08DP05

Low voltage 8-bit constant current LED sink driver with output error detection for automotive applications

Datasheet - production data

TSSOP16
(Exposed pad)

Features

- AECQ100 qualification
- Low voltage power supply down to 3 V
- 8 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- Able to drive 3.3 V microcontroller
- Output current: 5-100 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection 2.5 kV HBM

Applications

- Dashboard and infotainment backlighting
- Exterior/interior lighting
- DTRLs

Description

The STAP08DP05 is a monolithic, low voltage, low current power 8-bit shift register designed for LED panel displays. The STAP08DP05 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. In the output stage, eight regulated current sources are designed to provide 5-100 mA constant current to drive the LEDs.

The detection circuit checks 3 different conditions that can occur on the output line: short to GND, short to V_O or open line. The data detection results are loaded in the shift register and shifted out via the serial line output.

STAP08DP05 detection functionality is implemented without increasing the pin number. Through a secondary function of the output enable and latch pin (DM1 and DM2 respectively), a dedicated logic sequence allows the device to enter or leave detection mode. Through an external resistor, users can adjust the output current of the STAP08DP05, thus controlling the light intensity of the LEDs. In addition, the user can adjust the intensity of the brightness of the LEDs from 0% to 100% through the OE/DM2 pin.

The STAP08DP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, also satisfies the system requirement of high volume data transmission. The 3.3 V of voltage supply is very useful for applications that interface any microcontroller from 3.3 V. Compared with a standard TSSOP package, the TSSOP exposed pad increases the capability of heat dissipation by a factor of 2.5.

Table 1. Device summary

Order code	Package	Packing
STAP08DP5XTTR	TSSOP16 exposed-pad (Tape and reel)	2500 parts per reel

4.2 Construction note

	P/N M74HC365YTTR	P/N M74HC4851YTTR	P/N LM2902YPT	P/N SUP06	P/N STAP08DP05XTTR
Wafer/Die fab. information					
Wafer fab manufacturing location	ST Singapore			ST Catania	
Technology	High Speed CMOS	HCMOS4	Bipolar	BCD6S	BCD6
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	Cr/Ni/Au	Lapped Silicon
Die size (microns)	1828 x 1476 µm	1300 x 1212 µm	1430 x 1360 µm	2346x2116 µm	1588 x 1058 micron
Bond pad metallization layers	AlSi	AlSi	AlSiCu	AlCu	AlCu
Passivation type	PVAPOX/NITRIDE	PSG + NITRIDE	P-VAPOX/NITRIDE	TEOS+SiN+Polyimide	TEOS/SiN/Polyimide
Assembly information					
Assembly site	Amkor Philippines				
Package description	TSSOP16		TSSOP14	HTSSOP16	
Molding compound	Sumitomo G700LS				
Frame material	Cu				
Die attach process	Epoxy Glue				
Die attach material	ABLEBOND 8290				
Wire bonding process	Thermosonic ball bonding				
Wires bonding materials/diameters	Au 1 mil			Au 1.2mils	Au 1 mil
Lead finishing process	electroplating				
Lead finishing/bump solder material	Matte tin				

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	High speed CMOS/TSSOP16	R365	Assy lot 318860000
2	HCMOS4/TSSO16	R851	Assy lot 335234900
3	Bipolar / TSSOP14	0124	Assy lots A3L1630MS0474/ A3L1630MS0475/ A3L1630MS0476/ A3L1630MS0477/ A3L1630MS0478/ A3L1630MS0479
4	Bipolar / TSSOP14	0124	
5	Bipolar / TSSOP14	0124	
6	BCD6S/HTSSOP16	UP06	7B906226
7	BCD6S/HTSSOP16	UP06	7B918238
8	BCD6S/HTSSOP16	UP06	7B933263
9	BCD6S/HTSSOP16	UP06	7B617462
10	BCD6/HTSSOP16	UP04	ARI0*UP04ABA

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1 R365	Lot 2 R851	Lot 3 0124	Lot 4 0124	Lot 5 0124	
HTB/ HTOL	N	JESD22 A-108	Ta = 125°C, BIAS		168 H	0/77	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	0/77	0/77	0/77	
					500 H	0/45	0/45	0/77	0/77	0/77	
					1000 H	/045	0/45	0/77	0/77	0/77	
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77	0/77	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	0/77	0/77	0/77	
					300 cy	0/77	0/77	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	0/77	0/77	
					1000cy			0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	0/77	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	0/77	
Other Tests											
ESD	N	AEC Q101-001, 002 and 005	CDM			0/3 (1kV)	0/3 (1kV)				

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 6 UP06	Lot 7 UP06	Lot 8 UP06	Lot 9 UP06	Lot 10 UP04	
HTB/ HTOL	N	JESD22 A-108	Ta = 125°C, BIAS		168 H	0/40	0/40	0/77		0/77	
					500 H	0/40	0/40	0/77		0/77	
					1000 H	0/40	0/40	0/77			
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/77		0/77		0/45	
					500 H	0/77		0/77		0/45	
					1000 H	0/77		0/77			
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77		0/77		0/77	
					168H	0/77		0/77		0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77		0/77	0/77	0/77	
					300 cy	0/77		0/77	0/77	0/77	
					500 cy	0/77		0/77	0/77		
					1000cy	0/77		0/77			
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	0/40	0/40	0/40	0/40	0/77	
					500 H	0/40	0/40	0/40	0/40	0/77	
					1000 H	0/40	0/40	0/40	0/40		
Other Tests											
ESD	N	AEC Q101-001, 002 and 005	CDM								
						0/3 (500V)			0/3 (500V)	0/3 (500V)	

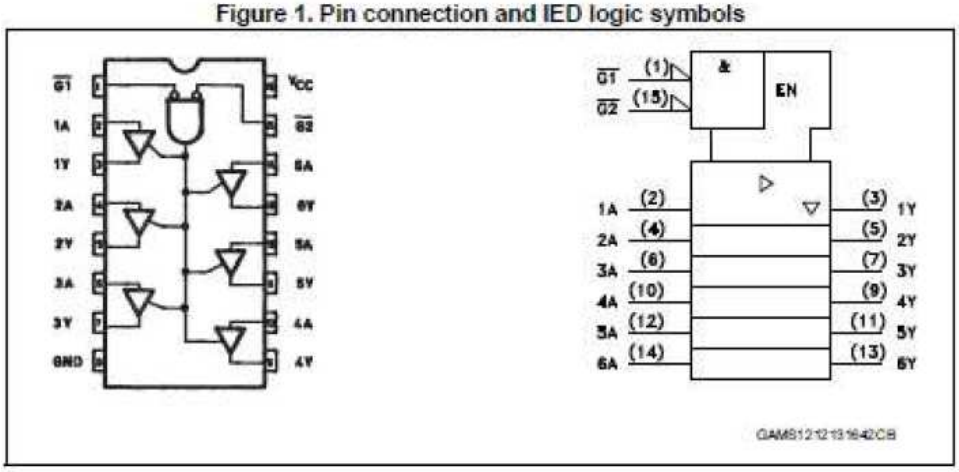
6 ANNEXES

6.1 Device details

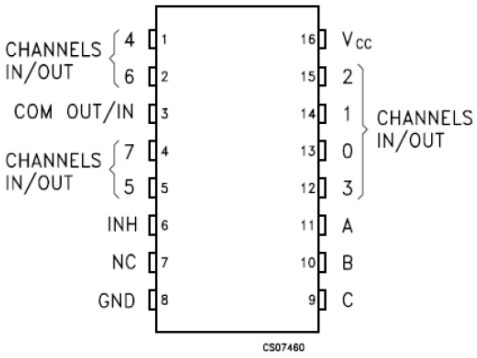
6.1.1 Pin connection

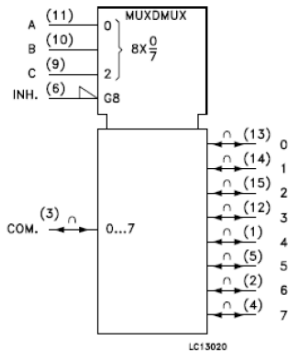
R365

Figure 1. Pin connection and IED logic symbols



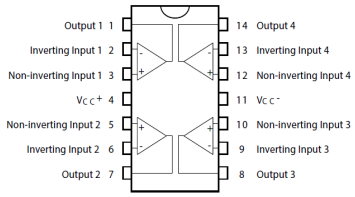
R851



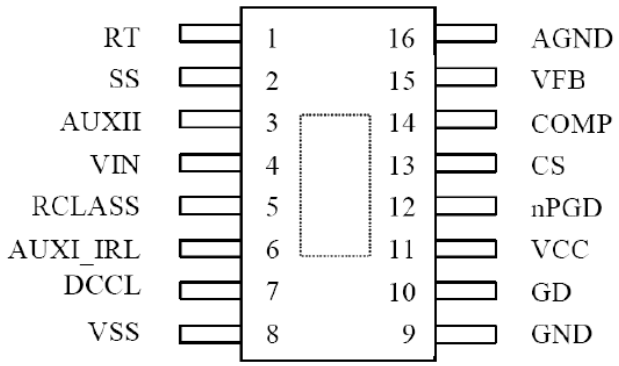


0124

Pin connections
(Top view)



UP06


RT
SS
AUXII
VIN
RCLASS
AUXI_IRL
DCCL
VSS
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
AGND
VFB
COMP
CS
nPGD
VCC
GD
GND

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.